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Parallel Computing: Architectures, Algorithms and Applications

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Preface

Parallel processing technologies have become omnipresent in the majority of new processors for a wide spectrum of computing equipment from game computers and standard PC's to workstations and supercomputers. The main reason for this trend is that parallelism theoretically enables a substantial increase in processing power using standard technologies. This results in a substantial reduction in cost compared to that of developing specialised high-performance hardware. Today the processing capacity of a desktop PC with a multi-core processor supersedes the compute power of a supercomputer of two decades ago at a fraction of the cost.

The utilisation of such powerful equipment requires suitable software. In practice it appears that the construction of appropriate parallel algorithms and the development of system and application software that can exploit the advantages of parallel hardware is not a simple matter. These problems have been studied for nearly five decades and, although much progress was made in the areas of parallel architectures, algorithm and software design, major problems remain to be addressed. The increasing replication of processing elements on chips and the use of standard components (COTS) for the relatively easy assembly of parallel systems comprising of a large number of processors (MPP) to achieve hitherto unachievable processing capacities, highlight the problems associated with the utilisation of these. Combined with the fast growth in the number of multi-core processors for PC's there is an increasing need for methods and tools to support the development of software to effectively and efficiently utilise parallel structures.

The international Parallel Computing conference series (*ParCo*) reported on progress and stimulated research in the high speed computing field over the past quarter century. New research results and techniques associated with the development and use of parallel systems were discussed at *ParCo2007*. This international event brought together a number of the top researchers in the field of parallel computing. Their research interests covered all aspects from architectures and networks to software engineering and application development. The use of FPGA's (Free Programmable Gate Arrays) was discussed in the same vein as the development of software for multi-core processors. Papers on a wide variety of application areas using high performance computers were presented. In contrast to software for specialised high speed computing applications, where specialists spend considerable time to optimise a particular piece of code, the challenge for the future is to make software development tools available that allow non-specialists to develop 'good' parallel software with minimum effort. All of these areas are in dire need of fundamentally new ideas to overcome the limitations imposed by existing paradigms.

In addition to the contributed papers a total of five mini-symposia on special topics and an industrial session formed part of the program. Prior to the conference two well attended tutorials were offered.

As with all previous conferences in this series the emphasis with the publication of the proceedings of *ParCo2007* was on quality rather than quantity. Thus all contributions were reviewed prior to and again during the conference. Organisers of mini-symposia were given the option to publish reviewed papers presented at the conference in these proceedings. In total two invited papers, 63 contributed papers and 26 papers from mini-symposia are included in this book.

The Editors are greatly indebted to the members of the International Program Committee as well as the organisers of the mini-symposia for their support in selecting and reviewing the large number of papers. The organisers of the conference are also greatly indebted to the members of the various committees for the time they spent in making this conference such a successful event. Special thanks are due to the staff of the Jülich Supercomputing Centre at Research Centre Jülich and the Institute for Scientific Computing, RWTH Aachen University for their enthusiastic support.

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